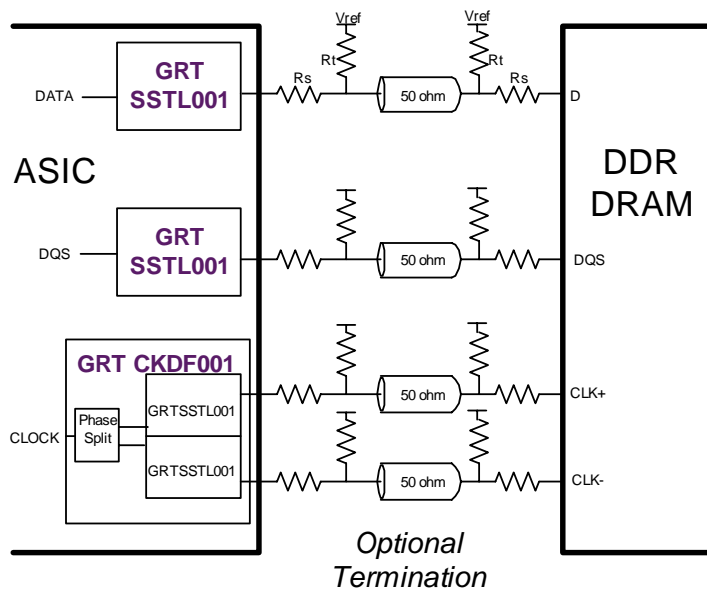


SSTL001, CKDF001

408 MBPS SSTL2 I/O BUFFER AND DIFFERENTIAL CLOCK DRIVER

SSTL001 & CKDF001 IN THE SYSTEM



APPLICATIONS

- DDR-DRAM data rates up to 408 Mbps
- General purpose SSTL2 interfaces
- Differential clocks up to 204 MHz

FEATURES

SSTL001 I/O Buffer

- ✓ 408 Mbps data rate
- ✓ Low duty cycle distortion
- ✓ Low Data-Dependent Jitter
- ✓ Improved drive strength
- ✓ Termination resistors optional
 - *potential for system cost savings*
- ✓ Equivalent area of TSMC PSSTL22X cell

CKDF001 Differential Clock Driver

- ✓ All improvements of the GRTSSTL001 cell
- ✓ 204 MHz operation
- ✓ Integrated phase splitter for ASIC single-ended clock compatibility and 408 Mbps performance
- ✓ Low sensitivity to common mode noise and general interference
- ✓ Tight duty cycle
- ✓ Equivalent area of two TSMC PSSTL22X cells

INTRODUCTION

The Greyrock Technology SSTL001 and CKDF001 I/O cells are designed in the TSMC CL013G process and are based on the TSMC PSSTL22X I/O buffer. The SSTL001 and CKDF001 form a sub-system for SSTL2 operation up to 408 Mbps data rates, providing improved design margin to interface to DDR-DRAM and other SSTL2-compatible devices.

The SSTL001 I/O Buffer operates to 408 Mbps with sufficient drive strength and margin such that termination is optional and may be eliminated for many applications.

The CKDF001 is a 204 MHz SSTL2 differential clock driver composed of dual GRTSSTL001 drivers with an integrated phase splitter, simplifying the ASIC designer's task of achieving 400+ Mbps performance. The CKDF001 provides the benefits of differential operation: low noise sensitivity with less duty cycle variation.

SSTL001 I/O buffers are used in the CKDF001 clock driver in order to meet DDR-DRAM 45-55% duty cycle requirements.

ELECTRICAL SPECIFICATIONS

Specification	Min	Nom	Max	Units	Note
VDD25	2.25	2.5	2.75	V	At ASIC
VDD12	1.08	1.2	1.32	V	At ASIC
Temperature	-10	27	125	C	Junction
Data Rate	0		408	Mbps	Maximum frequency is 204 MHz
Duty Cycle (clock)	45.8		52.0	%	50 Ω termination
	43.5		52.9	%	No termination
Bit Period Width (due to Data Dependent Jitter)	45.3		56.1	%	50 Ω termination, worst-case bit width as percent of period
	45.9		58.8	%	No termination, worst-case bit width as percent of period

DESIGN METRICS

The following describes design constraints and performance metrics.

- A data rate increase from 266 to 408 Mbps reduces the bit period by 53%, lowering the available settling time margin.
- Clock versus data timing margin is critical for proper data reception. Error sources such as setup and hold time, jitter, and lane skew all reduce this margin. When the margin becomes negative, bit errors will occur.
- Clock duty cycle distortion and Data-Dependent Jitter (DDJ), exacerbated by large board loads, small bit periods, and internal pad skews, contributor further to timing margin loss.

Given the reduced bit period at the 408 Mbps data rate, duty cycle distortion and DDJ were reduced in the SSTL001. This was accomplished by reducing internal signal path skews and increasing overall drive strength. For a baseline measurement, the PSSTL22X I/O pad was simulated at 408 Mbps with board loads, package models, and no termination. The SSTL001 was simulated under the same conditions. Table 1 compares the simulation results.

The SSTL001’s clock duty cycle and DDJ were reduced. The positive timing margin of +650 ps shows that bit errors will not occur using the SSTL001 at the required 408 Mbps data rate.

Operating parameters		Units		SSTL performance and board constraints.
Bit rate	408	Mbps		
Data bit period	+2450	ps		
Lane skew	-240	ps		
Setup time	-400	ps		
Hold time	-400	ps		
Design performance	PSSTL22X	SSTL001		Focus of design improvements
Cycle-to-Cycle Jitter	X	-10	ps	
Clock Duty Cycle	X	-320	ps	
Data Dependent Jitter	X	-430	ps	
Timing Margin	X	+650	ps	Sum of operating parameters and design performance

Table 1 – Worst-case Timing Margins at 408 Mbps (no termination)

Clock duty cycle and DDJ are summarized in Table 2, indicating the specific range of values expected from these two

Specifications subject to change without notice.

error contributors. The magnitude of the largest skew for each specification in Table 2 is consistent with the duty cycle and DDJ results of Table 1. The SSTL001 skews are listed in terms of percentage in the Electrical Specifications.

Specification	Buffer	Min	Max	Abs max	Units	Note
RX Duty Cycle Skew (CLOCK)	SSTL001	-320	142	320	ps	The amount the duty cycle skews, in ps, from the ideal 50% value. The 50% point is 2450 ps centered in a 4900 ps clock period (204 MHz). The critical parameter is the absolute maximum variance to either side of center.
					ps	
RX DDJ (DATA)	SSTL001	-201	430	201	ps	The amount the bit period changes relative to the ideal 2450 ps half-period. This condition could occur on the first 0 after a series of 1's. The critical parameter is the absolute maximum variance to either side of center.
					ps	

Table 2 – Duty cycle and DDJ specifications

Optional Termination

The design improvements of the SSTL001 buffer allow un-terminated transmission line operation for typical device package design, trace lengths and impedance tolerances. Use of 50 Ω termination resistors allows for operation at extended distances under wider PCB tolerances.

AVAILABILITY

The Greyrock Technology SSTL001 buffers and CKDF001 clock driver have been nominally verified in silicon as of April 1, 2004.

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